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CROSS SWITCH SUPPORTING SIMULTANEOUS DATA TRAFFIC IN OPPOSING DIRECTIONS

Field of the Invention

The present invention relates to a data transmission generally and, more particularly, to a cross switch supporting simultaneous data traffic in opposing directions.

Background of the Invention

Referring to FIG. 1, a conventional system 10 with several components A-D is shown. The system 10 transfers data on a shared bus 20. A path 22a illustrates data moving from a transmitter (i.e., component A) to a receiver (i.e., component B). The components A-D can behave as either a transmitter or a receiver, but not both simultaneously. For example, a path 22b illustrates data moving from a transmitter (i.e., component B) to a receiver (i.e., component A). The paths 22c and 22d show similar configurations of the component C and the component D. There may be a period of time for a particular one of the components A-D to

switch from being a receiver to transmitter, and vice versa. That period of time is measured in idle cycles of a system clock.

For example, a bus structure can multiplex addresses and a data over the bus 20. With such an implementation, the component A can read from the component B by first sending an address over the bus 20. The component B receives the address, decodes the address information, fetches the requested data, and sends the requested data back on the bus 20. The sequence of operations described creates the bus idle cycles where other components do not have access to the bus 20.

During the bus idle cycles, if the component C needs to read from the component D, the bus 20 is not available. In addition, the bus 20 normally only runs at one clock frequency. All of the components A-D need to interface to the bus 20 at the frequency of the bus 20. Conventional solutions resolve such multiple bus requests by waiting for the bus 20 to be available by adding idle cycles to separate the bus activity.

It would be desirable to implement a bus that implements simultaneous data traffic in opposing directions without imposing idle cycles.

Summary of the Invention

The present invention concerns an apparatus comprising a first bus segment, a second bus segment and a switch. The first bus segment may be configured to transfer data in either a first direction or a second direction. The second bus segment may be configured to transfer data in either the first direction or the second direction. The switch may be connected between the first bus segment and the second bus segment. The switch may be configured to transfer data in both the first direction and the second direction simultaneously.

The objects, features and advantages of the present invention include providing a switch that may (i) support simultaneous data traffic in opposing directions, (ii) reduce idle cycles, (iii) increase bus bandwidth and performance and/or (iv) support components that run at different bus frequencies.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a diagram illustrating a conventional bus configuration;

FIG. 2 is a diagram illustrating a preferred embodiment of the present invention; and

FIG. 3 is a more detailed diagram illustrating the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 2, a diagram of a system 100 is shown in accordance with the preferred embodiment of the present invention. The system 100 generally comprises a bus 120, a switch 130 and a number of components A-D. In one example, the switch 130 may be a cross switch (or switch box). The switch 130 generally comprises a portion (or buffer) 140 and a portion (or buffer) 150. The portion 140 may accommodate bus traffic in one direction, while the portion 150 may accommodate bus traffic in another direction. For example, traffic from the component C to the component D may be transferred along the first portion 140. Traffic from the component A to the component B may be transferred along the second portion 150. The first portion 140 may be implemented as a number of memory cells 142a-142n. The second portion 150 may be

implemented as a number of memory cells 152a-152n. The first portion 140 and the second portion 150 may be implemented as first-in, first-out (FIFO) buffers.

The switch 130 may be implemented between segments of the bi-directional bus 120. A first segment 160a may be implemented on one side of the switch 130. A second segment 160b may be implemented on another side of the switch 130. The switch 130 may be inserted between the first segment 160a and the second segment 160b. While two segments are shown connected to the switch 130, additional segments may be connected to meet the design criteria of a particular implementation. The component A and the component D may be connected to the segment 160a. The component B and the component C may be connected to the segment 160b. When the component A is requesting data (e.g., REQUESTA) from the component B, the component C is allowed to request data (e.g., REQUESTC) from the component D. The switch 130 will then normally transfer the data request REQUESTA from segment 160a to the segment 160b, and the data request REQUESTC from the segment 160b to the segment 160a, simultaneously.

When the component B receives the data request REQUESTA, the component B takes the idle cycles to fetch data (e.g., DATAB).

At the same time, the component D may have received the data request REQUESTC. The component D may also use the respective idle cycles to fetch the data DATAD. The component B and the component D put respective data on segment 160b and the segment 160a of the bus 130. Again, the switchbox 130 forwards the data DATAB to the segment 160a and the data DATAD to the segment 160b at the same time.

Furthermore, the component A and the component C do not necessarily have to make the appropriate data requests simultaneously. Similarly, the data DATAB and the data DATAD do not necessarily have to be put on the respective segment of the bus 130 simultaneously. The switch 130 may be implemented as two buffers 140 and 150. The buffer 140 may connect one input from the segment 160a and present an output to the segment 160b. The buffer 150 may operate in the reverse direction. The switch 130 holds the data that arrives early, waits for the other segment (e.g., the segment 160a or the segment 160b) to be available, then presents data from one segment (e.g., the segment 160a) to the other segment (e.g., 160b).

The switch 130 may hold data from one segment (e.g., 160a) before forwarding the data to the other segment (e.g., 160b).

The size (e.g., depth and width) of the buffers 140 and 150 may be adjusted to meet the design criteria of a particular implementation. The switch 130 may also allow simultaneous access from two independent components (e.g., the components A and D) to two other components (e.g., the components B and C). In one example, the segment 160a and the segment 160b may operate at the same frequency. In another example, the segment 160a may operate at a first frequency and the segment 160b may operate at a second frequency. The first frequency may be the same, greater than or less than the second frequency.

The system 100 may be extended into multiple segments with multiple buffers and forwarding logic. The system 100 may (i) reduce idle cycles, (ii) increase bus bandwidth and performance, (iii) support components that run at different bus frequencies. The system 100 may be implemented generically and be used in any shared bus architecture, be in systems or VLSI chips.

Referring to FIG. 3, a more detailed diagram of the system 100 is shown. In particular, additional details of the switch 130 are shown. For example, a control portion 170a is shown between the buffer 140 and the bus segment 160a. A control portion 170b is shown connected between the buffer 150 and the bus segment

160b. The control portion 170a generally comprises a switch portion 172a and a control logic portion 174b. Similarly, the control portion 170b generally comprises a switch portion 172b and a control logic portion 174b.

The control logic portion 174a may receive a bus busy signal (e.g., BUSY) from the bus segment 160a. The signal BUSY generally indicates if the bus segment 160 has traffic (e.g., data, addresses, etc.). The control portion 170a allows data to be transferred from the buffer 140 to the bus segment 160a by closing the switch 172a if the signal BUSY indicates that the bus segment 160a is not busy. If the signal BUSY indicates that the bus segment 160 is busy, then the control portion 170a opens the switch 172a, not allowing data to be presented from the buffer 140. The control portion 170b provides similar operation while the control portion 170a is shown with a switch 172a, other components may be implemented to meet the design criteria of a particular implementation. For example, a tri-state buffer may be implemented to control data flow. The buffer 140 may load information from the bus segment 160b while the buffer 150 loads information from the bus segment 160a. Information (e.g., data, addresses, etc.) may be unloaded from the buffer 140 once the bus segment 160a is

not busy. Similarly, data may be unloaded from the buffer 150 once the bus segment 160b is not busy. Portions of data may be loaded and/or unloaded from the buffers 140 and 150 at different times. For example, if the component A needs to send a large piece of data to the component B, a first portion of the data can be loaded into the buffer 140 while a smaller portion of data is being loaded from the component C to the buffer 150. The buffer B may start unloading data to the bus segment 160b, which may interrupt the data being loaded into the buffer 140. After the data is unloaded from the buffer 150, additional data may be loaded into the buffer 140.

As used herein, the term "simultaneously" is meant to describe events that share some common time period but the term is not meant to be limited to events that begin at the same point in time, end at the same point in time, or have the same duration.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.